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FPGA IMPLEMENTATION OF MAC UNIT USING VEDIC MULTIPLIER

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Abstract—
Implementation of MAC unit is essential for any ALU or microprocessor based application specific integrated circuit. Thus implementing such a circuit with either high speed or low power is very essential for the proper operation of the MAC unit. The MAC unit implemented has slower speed due to inefficient implementation of the multiplier. Ancient Indian mathematics proposed a Vedic technique which allows us to implement the Vedic based multiplier on hardware. This multiplier is not only hardware friendly but also improves the speed of operation of the MAC unit. If a MAC unit is used N times in a microprocessor based system and we are able to speed up the multiplier by a factor of K then the overall speed improvement during the given time is NK.In the previous papers the MAC unit implemented has slower speed due to inefficient implementation of the multiplier .The Vedic multiplier is not only hardware friendly but also improves the speed of operation of the MAC unit .Instead of simple Vedic multiplier, in this paper we will be using a parallel or pipelined Vedic multiplier which will give faster outputs than the previous papers.

Keywords—MAC,Vedic Multiplier,Vedic mathematics, high speed and low power,Urdhava Tiryakbhyam Sutra,pipeline.

I.INTRODUCTION

Due to fast growth of transferable electronic systems like laptop, calculator and mobile etc., and the low power devices has become extremely essential in today's community. The Low power and high throughput circuitry design are playing the challenging role in VLSI designing for real-time signal processing. A high speed and high throughput MAC unit is always a key to attain a high level performance in digital signal processing system. The main motivation of this work is to explore different pipelined multiplier and accumulator structure and circuit design techniques which are suitable for implementing high output in signal processing algorithms and at the same time achieve low power consumption. A regular MAC unit contains of multipliers and accumulators that have the sum of the previous consecutive products. In this paper a high performance and a high throughput MAC unit with Vedic multiplier and pipe lined accumulator is proposed. Digital signal processors (DSPs) are very essential in different engineering disciplines and the speed of the DSPs is determined by the speed of its MAC Unit.Fast multiplication is very important for convolution, Fourier transforms etc. A fast method for multiplication based on ancient Indian Vedic mathematics is proposed in this paper. Out of the 16 sutras of Vedic mathematics the Urdhva Triyagbhyam Sutra implemented because this sutra is applicable to all cases of algorithm for n×n bit numbers and gives minimum delay for multiplication of all types of numbers. It enables parallel generation of partial products and eliminates unwanted multiplication steps. Instead, we focus on bringing high performance with new levels of reuse and portability for the logic designer. We have modeled our architectures in VHDL and analyze achievable performance within a real life application as it is being increasingly used for variety of computationally demanding. The function of the MAC unit is given by the following equation $F = \Sigma Ai X Bi$.

The paper is organized as follows. Section II presents the Basic operation and design of MAC architecture. Vedic Multiplier and Comparative result described at Section III and IV respectively and Section V shows the conclusion ofthe work.

II. MAC ARCHITCHTURE

The multiplication and accumulation is the main computational kernel in Digital Signal Processing architectures. The MAC unit determines the speed of overall System as it is always lies in the critical path. To develop high Speed MAC unit essential for real time DSP application. In Order to improve the speed of the MAC unit there are two Major factors that need to be considered. The first one is the

Fast multiplication network and the second one is the Accumulation. Both of these stages require addition of large Operands that involve long paths for carry propagation. In Recent MAC accumulation and addition are merging to save The time and power. The MAC unit basically do the Multiplication of two Numbers multiplier and multiplicand and add that product in result stored in the accumulator. For high speed MAC unit, faster adder and multiplier circuits are Required. Figure 1 shows the MAC unit architecture A basic MAC unit can be divided into two main blocks.

1. Multiplier
2. Accumulator

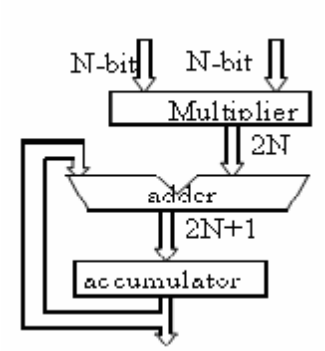

Fig.1.MAC unit basic structure

The design of MAC unit architecture from Figure 1 shows that the design consists of multiplier, accumulator using carry look Ahead adder (CLA). In this paper, Vedic multiplier and carry Look adder, and full pipelined accumulator are used to high Performance MAC unit design. Vedic multiplier is used to Multiply the two N-bit number. Given multiplier also reduces Power consumption of the MAC unit. The inputs for the MAC Are fetched from memory location and fed to Vedic multiplier block of the MAC which will perform multiplication and give the result to adder which will accumulate the result and then will store the result into a memory location. This entire process is to be achieved in a single clock cycle [2].

III.VEDIC MULTIPLIER

The use of Vedic mathematics lies in the fact that it reduces the typical calculations in conventional mathematics to very Simple one. This is so because the Vedic mathematics are accepted to be based on the natural principles on which the Human mind works**.** The proposed Vedic multiplier is based on the Vedic multiplication Sutras or formulae. These methods Have been traditionally used for the multiplication of two numbers in the decimal number system. In this paper we apply The same ideas to the binary number system to make the proposed algorithm compatible with the digital hardware. Vedic multiplication based on *URDHVA TIRYAKBHYAM SUTRA* algorithms discussed below.

URDHVA TIRYAKBHYAM SUTRA

Urdhva Tiryakbhyam is a Sanskrit term which means "Vertically and crosswise" of ancient Indian Vedic Mathematics. Urdhva Tiryakbhyam Sutra is a general Multiplication formula applicable to all cases of multiplication. The idea here is based on a concept which results in the generation of all partial products along with the concurrent addition of these partial products in parallel. The parallelism in generation of partial products and their summation is obtained using Urdhva Tiryakbhyam explained in Figure blow. Since there is a parallel generation of thepartial products and their sums the processor becomes independent of the clock frequency. Thus the multiplier will need the same amount of time to calculate the product and hence is independent of the clock frequency. The Vedic multiplier has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other multipliers, thereby making it time, space and power efficient. To illustrate this multiplication scheme, let us consider the multiplication of two decimal numbers (325 * 738). Line diagram for the multiplication is shown in Figure 2. Initially the LSB digits on the both sides of the line are multiplied and added with the carry from the previous step. This generates one of the bits of the result and a carry. This carry is added in the next step and the process goes on likewise. If more than one line are there in one step, all the results are added to the previous carry. In each step, least significant bit act as the result digit and all other digits act as carry for the next step. Initially the carry is taken to be zero.

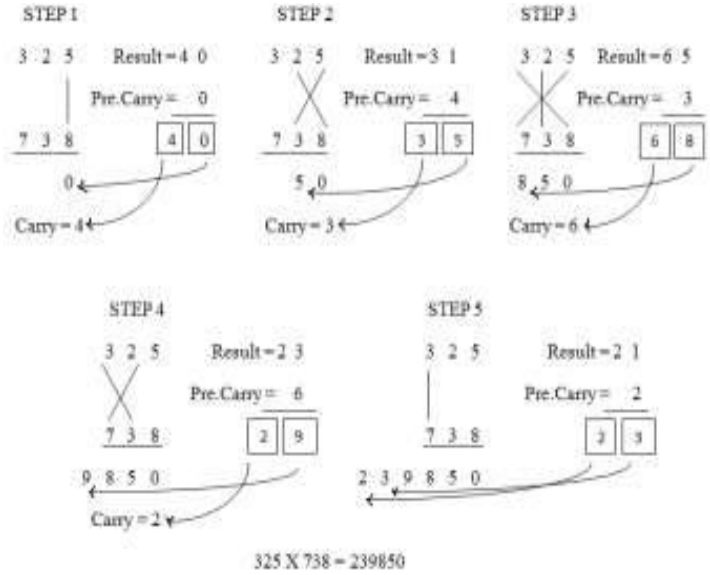

Fig. 2. Multiplication of two decimal numbers by Urdhva Tiryakbhyam

Firstly, least significant bits are multiplied which gives the Least significant bit of the product (vertical). Then, the LSB of The multiplicand is multiplied with the next higher bit of the Multiplier and added with the product of LSB of multiplier and next higher bit of the multiplicand (crosswise). The sum

gives second bit of the product and the carry is added in the output of next stage sum obtained by the crosswise and vertical multiplication and addition of three bits of the two numbers from least significant position. Next, all the four bits are processed with crosswise multiplication and addition to give the sum and carry. The sum is the corresponding bit of the product and the carry is again added to the next stage Multiplication and addition of three bits accept the LSB. The Same operation continues until the multiplication of the two MSBs to give the MSB of the product

IV. COMPARATIVE RESULTS OF PROPOSED VEDIC MULTIPLIER FOR MAC UNIT

To show the efficiency of proposed Vedic multiplier for MAC unit, it has been implemented and compared with other popular multiplier structures based on different multiplication algorithms on the same platform of target FPGA, which has been used to implement these popular multiplier structures. Comparison tables are shown below:-

In the following given table which target FPGA has been used belongs to Virtex 2P (family), XC2VP2 (device), FG 256 (Package), -7 (speed grade).

Table 1: Comparative table

Maximum Combinational Path Delay (in ns) for different multipliers at eight bit level						
Karatsuba [19]	Vedic Karatsuba [19]	Modified Booth-Wallace [21]	Vedic with partitioning [21]	Conventional Vedic [19]	Vedic with CSA [12]	Vedic multiplier [4]
31.029	18.695	15.815	15.685	15.418	13.07	11.886

In the following given table which target FPGA has been used belongs to Spartan 3 (family), XC3S50 (device), PQ 208 (Package), -4 (speed grade).

Table 2: Comparative table

Maximum Combinational Path Delay (in ns) for different multipliers at eight bit level			
Array [13]	Booth [13]	Conventional Vedic [13]	Vedic multiplier [4]
32.01	29.549	24.16	19.467

In the following given table the target FPGA used belongs to Virtex 2P (family), XC2VP2 (device), FG 256 (Package), -7 (speed grade).

Table 3: Comparative table

Maximum Combinational Path Delay (in ns) for different multipliers at different bit levels							
N bit level multiplier	Karatsuba [19]	Vedic Karatsuba [19]	Modified Booth-Wallace [21]	Vedic with partitioning [21]	Conventional Vedic [21]	Vedic with CSA [12]	Vedic Multiplier [4]
4-Bit	---	---	---	---	---	8.405	8.387
8-Bit	31.029	18.695	15.815	15.685	15.418	13.070	11.886
16-Bit	46.811	27.81	36.071	23.063	22.604	18.580	15.718
32-Bit	82.834	49.864	---	---	35.76	---	20.574

In the following given table the target FPGA used belongs to Spartan 3 (family), XC3S50 (device), PQ 208(Package),-4(speed grade).

Table 4: Comparative table

Maximum Combinational Path Delay (in ns) for different multipliers at different bit levels				
N bit level multiplier	Array [13]	Booth [13]	Conventional Vedic [13]	Vedic Multiplier [4]
8-Bit	32.01	29.549	24.16	19.467
16-Bit	60.928	70.809	36.563	29.012

By implementing the proposed Vedic multiplier for MAC unit on the same reconfigurable hardware as given make the platform (hardware) independent algorithmic technique and approach based comparison. So by this it can be concluded that the algorithm and approach which has been proposed to design MAC unit using proposed Vedic multiplier, in this research work, is better in comparison to the other popular algorithms.

V. CONCLUSION

We have proposed a design for the NxN bit MAC Unit using a unique Vedic multiplier which provides better results with respect to the conventional MAC unit .This Proposed MAC Unit is very useful for designing the high speed digital signal processors. And thus the optimized designs can be made for FFT, FIR, IIR etc.

An improved version of the conventional MAC unit has been designed and implemented in FPGA. This design can be used in Digital Signal Processors and in devices where power and area are major constraints. In the future, the delay can be further reduced by Introducing a pipelined architecture in the multiplier design.

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