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"Design and Implementation of single precision floating point multiplier with the help Xilinx on FPGA."

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ABSTRACT- : Floating point arithmetic is widely used in many areas. Multipliers play an important role in today's digital signal processing and various other applications. A system's performance is generally determined by the performance of the multiplier, This paper presents an efficient FPGA implementation of Single precision floating point multiplier using VHDL. The aim of project is design and simulation of a floating point multiplier that supports the IEEE 754-2008 binary interchange format, the proposed multiplier doesn't implement rounding and presents the significant multiplier.

Keywords- *SIGNIFICANT MULTIPLIER, VHDL SIMULATION*.

I. INTRODUCTION

Floating point numbers are one possible way of representing real numbers in binary format, the IEEE 754[1] standard presents two different floating point formats, Binary interchange format and Decimal interchange format.

The aim of project is design and simulation of a floating point multiplier that supports the IEEE 754-2008 binary interchange format, the proposed multiplier doesn't implement rounding and presents the significant multiplication result as is (48 bits).

Multiplying two numbers in floating point format is done by adding the exponent of the two numbers then subtracting the bias from their result, and multiplying the significant of the two numbers, and calculating the sign by XORing the sign of the two numbers.The way floating point operations are executed depends onthe data format of the operands. IEEE standards specify aset of floating point data formats, single precision and double precision. The Single precision consists of 32 bits and the Double precision consists of 64 bits.

Figure 1

I. shows the IEEE single and double precision data formats

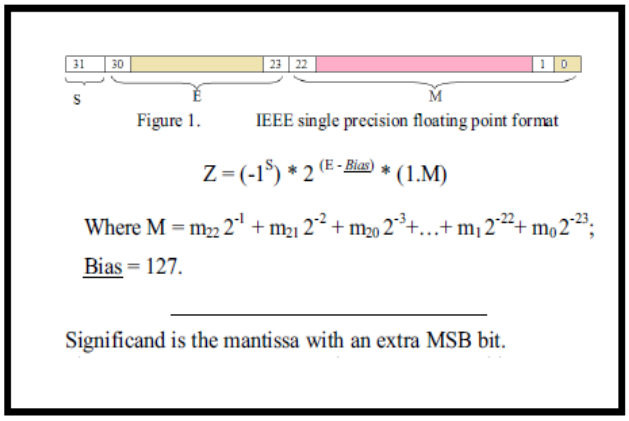


Figure 1. IEEE single precision floating point format

$$Z = (-1^{S}) * 2^{(E - \underline{Bias})} * (1.M)$$

Where $M = m_{22}2^{-1} + m_{21}2^{-2} + m_{20}2^{-3} + \ldots + m_{1}2^{-22} + m_{0}2^{-23}$;

Bias = 127.

Significand is the mantissa with an extra MSB bit.

II. Floating point multiplication algorithm

1. Add exponents
2. Multiply fractions
3. If product is 0, adjust for proper 0
4. Normalize product fraction
5. Check for exponent overflow or underflow
6. Round product fraction

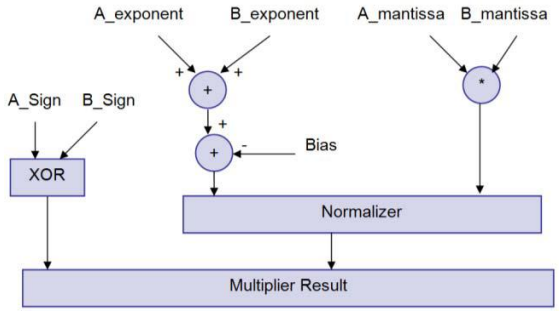
- Exponents 00000000 and 11111111 reserved
- Smallest value

- Exponent: 00000001
  Þ actual exponent = 1 – 127 = –126
- Fraction: 000…00 Þ significand = 1.0
- $\pm 1.0 \times 2^{-126} \approx \pm 1.2 \times 10^{-38}$

• Largest value
- exponent: 11111110
  Þ actual exponent = 254 – 127 = +127
- Fraction: 111…11 Þ significand ≈ 2.0

$\pm 2.0 \times 2^{+127} \approx \pm 3.4 \times$

II. PROPOSED PLAN



ROUNDING

e = -1	e = 0	e = 1
1.00 X 2^(-1) = 1/2	1.00 X 2^0 = 1	1.00 X 2^1 = 2
1.01 X 2^(-1) = 5/8	1.01 X 2^0 = 5/4	1.01 X 2^1 = 5/2
1.10 X 2^(-1) = 3/4	1.10 X 2^0 = 3/2	1.10 X 2^1= 3
1.11 X 2^(-1) = 7/8	1.11 X 2^0 = 7/4	1.11 X 2^1 = 7/2

III. SYSTEM REQUIREMENT

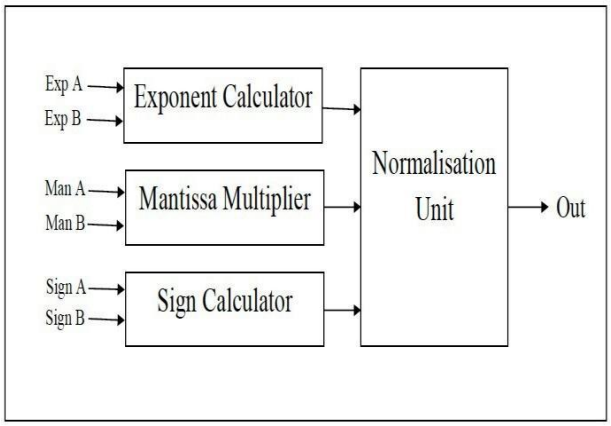
- ***Software Requirement***

Operating System: Windows XP/7
Language/Technology: VHDL
Tools: Xilinx ISE 14.5

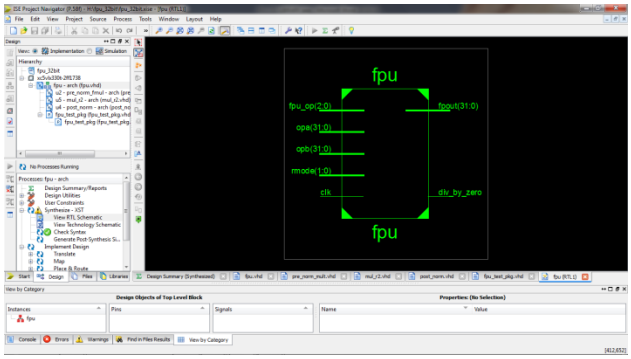
- ***Hardware Requirement***

Spartan 3 FPGA

IV. SYSTEM ARCHITECTURE



V. RTL schematic



VI. CONCLUSION

This paper presents design and simulation of a floating point multiplier that supports the IEEE 754-2008 binary interchange format, The proposed multiplier doesn't implement rounding and presents the significand multiplication result as is (48 BITS), This gives bitter precision if the whole 48 bits are utilized in another unit; i.e with a floating point adder to form a MAC Unit. But The floating point multiplier core generated by Xilinx core generated by Xilinx core generator does not indicates the 48 bits of mantissa due to rounding and is not beneficial in case DSP application of large dynamic range.

VII. *REFERENCES*

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